Single-Event Upset in Flash Memories [1]

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INTRODUCTION

Although hardened memories continue to be available for space applications, the need for large amounts of memory, lower cost, and reduced weight has caused many spacecraft to rely on unhardened commercial memory devices. For example, the Cassini spacecraft will use a solid-state recorder, fabricated with commercial DRAMs, to record science data. A similar recorder was used successfully on the Clementine mission[1]. These recorders use complex error-detection-and-correction architectures to overcome the inherent sensitivity of DRAMs to soft errors.

Flash memories are attractive to designers because they are nonvolatile. They have evolved rapidly, and are of considerable interest in small spacecraft for selected applications that can tolerate slow write operations compared to DRAMs. Flash memories are now available with 16-Mb and 32-Mb capacity. They are more straightforward to use than EEPROM, and their internal storage technology is far more resistant to single-event upset than DRAMs. However, flash memory architectures are complex, providing page-mode operations for faster access, and block-erase modes. They typically use an internal controller(state machine) with an instruction register, program counter, and register file, and thus combine many of the potential upset phenomena of microprocessors along with upset effects in the large internal memory array [2]. For example, a block diagram of the Intel 28CF016 flash memory is shown in Figure 1. The interface control logic block decodes system input signals to allow transparent operation of the memory in typical systems. The internal command-state and write-state machines, shown in bold outlines, control device operation and allow writing to be done at the byte or word level using internal page buffers (256 bytes). Erase operations can be done on entire blocks. The architecture also allows queuing of subsequent operations before the current operation is completed. Only about 1/2 of the chip area is used for the memory array in this device.

This paper discusses single-event upset effects in flash memories, using heavy ions at the Texas A&M cyclotron. Initial results are presented for one manufacturer that compare upset in the individual memory elements with the more complex functional failure modes that occur in the internal state machine and its control registers. This device is designed to function with either 5-V or 3.3-V power supply levels for read operations, but requires an additional 5 or 12-V power supply for write and erase operations. Testing was done only with a 12-V write voltage (because write operations are much faster), but with either 3.3 and 5 V voltages for the main power supply (both conditions were evaluated).

UPSET RESULTS AFFECTING CIRCUIT OPERATION

When the entire device was irradiated, several different types of functional errors occurred. The threshold LET for these functional errors was approximately 7 MeV-cm^2/mg. The cross section for functional errors was much smaller than that for memory upset, ranging between 10^{-7} and 10^{-6} cm^2 for the various error modes. The cross section remained at about this same order of magnitude even when ions with higher LET were used, indicating that the response is caused by upsets in a small localized region (or regions) of the microcontroller. The finite time period required to go through operational cycles to detect incorrect operation introduces a latency period that makes it difficult to determine the precise time at which the internal error occurred. This latency, combined with counting statistics, results in larger uncertainty in the cross section for this

[1]The research in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration, Code Q.

type of functional error than for conventional upsets involving arrays of registers or storage cells. However, the small cross sections are consistent with upsets in individual control bits or small control registers.

The functional error modes that were observed are shown in Table 1. In the majority of cases these functional conditions interfered with normal device operation and continued until power was temporarily removed from the device and reapplied, after which normal operation could be resumed. Most of these conditions did not change the contents of the internal memory array, but locked up the internal controller. However, one error type (designated "row/column changes") caused large portions of the array to be rewritten.

Table 1. Functional Error Modes Observed for the 28 F016SV Flash Memory

Error Type	Description	Recovery Method
Blink clear lockup	Block clear complete status never appears	Power cycling
False block clear	One or more blocks show block clear, even though they are not cleared	Power cycling
Slow block clear	Many passes are required to establish block clear for one or more blocks	Wait (power cycling not req.)
Row/column changes	Large portions of the memory array change state within a short time period, accompanied by block clear lockup	Power cycling
Slow first add. prog.	After successful block clear, the first address takes many passes and a long time to complete. Subsequent addresses work OK.	Wait
Read lockup	Status bits indicate internal modes and instructions are active, when device is expected to be in the ready state.	Power cycling
Write lockup	DATA WRITE status bit stuck in write-error mode during write sequence	Power cycling

In addition to functional interrupt conditions, a high-current condition was sometimes observed after the device was irradiated in a static mode (no read or write operations during irradiation). The power supply current was initially unchanged, but it increased to very high levels at specific, reproducible address locations during the read cycle that was initiated after the beam was turned off. The current at these address locations exceeded 200 mA, and caused one device to be destroyed. The high-current condition could be eliminated by power cycling. The reason for this response is not known at this time, but could be due to snapback [3,4], because, unlike latchup, it is only activated by specific electrical conditions that are applied after the beam was turned off. A more thorough investigation of this phenomenon will be presented in the final paper.

UPSET OF FLASH MEMORY CELLS

In order to separate effects in the microcontroller from memory upset, the microcontroller section of the memory was masked with 200 roils of copper. Figure 2 shows the location of the internal operating blocks, along with the section of the device that was shielded during tests of the

array. Input buffers, address latches, interface control logic, and address/timing decoding were all shielded by the mask. However, the high voltage circuits used to write and erase were not covered by the shield, nor were the sensing circuits. None of the functional abnormalities discussed earlier occurred when the shield was in place, and it was then possible to observe single-event upset in the memory array.

Memory upsets occurred at random address locations. Upsets were first observed at an LET of about 20 MeV-cm^2/mg. These results are shown in Figure 3. The upper curve shows results with a power supply voltage of 5 V. The lower curve shows results with a power supply voltage of 3.3 V, with a threshold of 44 MeV-cm^2/mg. Unlike most devices, this device is more susceptible to single-event upset when a high voltage (5 V) is used than when a low power supply voltage is used. The cross section for cell upset was very small compared to the total cell area, which may indicate that upset in the high-voltage section, used only during write and block-clear operations, was involved. Additional tests will be done for the full paper without the 12-V write/erase voltage applied (essentially simulating a read-only mode) to investigate this further.

DISCUSSION

The results of these tests have shown three general types of responses this particular flash memory: (1) upset effects in the memory cells, which only occur for LET> 20 MeV-cm^2/mg; (2) several types of functional abnormalities that are triggered by heavy ions, and do not occur when the controller section of the memory is shielded from heavy ions; and (3) a potentially destructive high-current condition at specific address locations.

The functional abnormalities appear to be caused by upset within the internal registers or the state machines themselves, because they do not occur when the controller sections of the device are shielded from the heavy-ion beam. The cross section for functional abnormal ities is low, corresponding to upset rates of= 10^{-3} per device per year in interplanetary space, and comparable or lower upset rates would be expected for most earth-orbiting satellites. However, the wide range of signatures would make it very difficult to deal with this type of upset in system applications. Many of the functional problems could only be determined during the complex write or erase cycles that are possible with these devices, and could gradually build up, undetected, if the device was used in a standby mode, which is a very likely condition for this type of memory. Although block errors in individual memories could be overcome by clever error-detection-and-correction architectures, these devices are clearly much more difficult to deal with than DRAMs because of the complex internal architecture. The high-current condition is of even greater concern, and needs to be investigated more thoroughly.

The results in this paper suggest that it will be difficult to use flash memories in a continuous active mode in space applications because of the functional errors that occur in the microcontroller. However, they may still be quite useful as nonvolatile memory, activating them only during restricted time periods.

The full paper will compare results for the Intel device with similar devices from Samsung and Toshiba that contain similar architectures, but use different cell technologies [5,6]. A more thorough characterization will be done for cell and functional upset modes, using additional ions and/or angles in order to provide more accurate information about the LET dependence.

References

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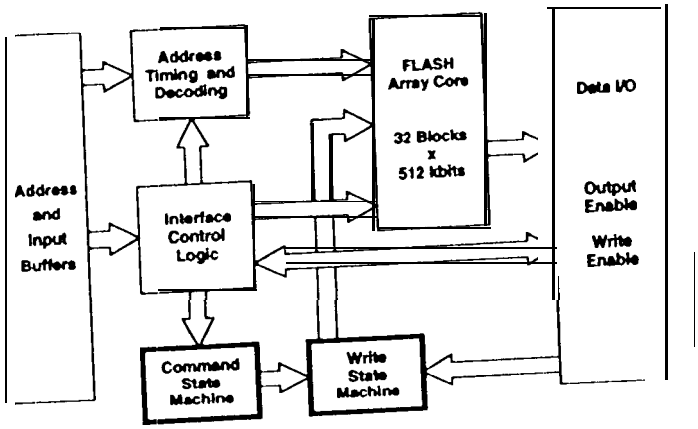

Figure 1. Block Diagram of the Flash Memory.

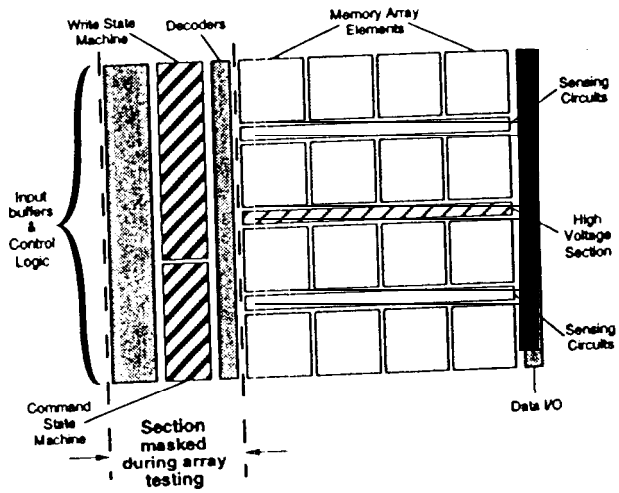

Figure 2. Physical Diagram of the Flash Memory Chip, Showing Microcontroller Region and Placement of Mask for Cell Upset Testing

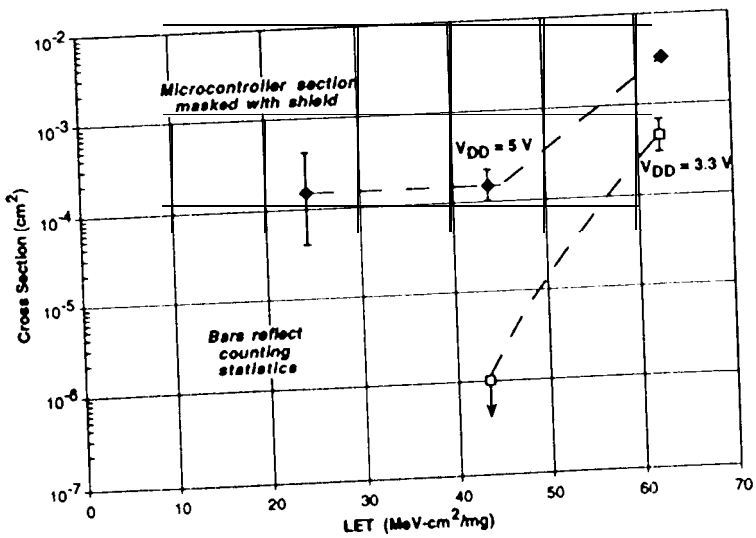

Figure 3. Dependence of Cell Upset Rate on LET (Microcontroller Section Shielded)